Most Frequently Occurring Classifications of Patents Returned
From A Search of 10085919 on June 15, 2004

Original Classifications
 14   714/726
  5   714/727
  5   714/729
  3   714/731
  2   324/158.1
  2   324/73.1
  2   327/199
  2   327/202
  2   714/728
  2   714/733

Cross-Reference Classifications
  9   714/733
  8   714/726
  5   324/73.1
  5   714/729
  4   714/724
  4   714/727
  4   714/731
  3   714/736
  2   324/158.1
  2   327/291
  2   327/299
  2   365/201
  2   712/220
  2   714/730
  2   714/732
  2   714/734
  2   714/739

Combined Classifications
 22   714/726
 11   714/733
 10   714/729
  9   714/727
  7   324/73.1
  7   714/731
  5   714/724
  4   324/158.1
  3   714/732
  3   714/736
  2   327/199
  2   327/202

2	327/291
2	327/299
2	365/201
2	712/220
2	714/728
2	714/730
2	714/734
2	714/738
2	714/739

Titles of Most Frequently Occurring Classifications of Patents Returne
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From A Search of 10085919 on June 15, 2004

22 714/726   (14 OR, 8 XR)
        Class   714 : ERROR DETECTION/CORRECTION AND FAULT
                          DETECTION/RECOVERY
        714/699   PULSE OR DATA ERROR HANDLING
        714/724   .Digital logic testing
        714/726   ..Scan path testing (e.g., level sensitive sca
n
                      design (LSSD))

11 714/733   (2 OR, 9 XR)
        Class   714 : ERROR DETECTION/CORRECTION AND FAULT
                          DETECTION/RECOVERY
        714/699   PULSE OR DATA ERROR HANDLING
        714/724   .Digital logic testing
        714/733   ..Built-in testing circuit (BILBO)

10 714/729   (5 OR, 5 XR)
        Class   714 : ERROR DETECTION/CORRECTION AND FAULT
                          DETECTION/RECOVERY
        714/699   PULSE OR DATA ERROR HANDLING
        714/724   .Digital logic testing
        714/726   ..Scan path testing (e.g., level sensitive sca
n
                      design (LSSD))
        714/729   ...Plural scan paths

 9 714/727   (5 OR, 4 XR)
        Class   714 : ERROR DETECTION/CORRECTION AND FAULT
                          DETECTION/RECOVERY
        714/699   PULSE OR DATA ERROR HANDLING
        714/724   .Digital logic testing
        714/726   ..Scan path testing (e.g., level sensitive sca
n
                      design (LSSD))
        714/727   ...Boundary scan

 7 324/73.1   (2 OR, 5 XR)
        Class   324 : ELECTRICITY: MEASURING AND TESTING
        324/73.1   PLURAL, AUTOMATICALLY SEQUENTIAL TESTS

 7 714/731   (3 OR, 4 XR)
        Class   714 : ERROR DETECTION/CORRECTION AND FAULT
                          DETECTION/RECOVERY

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                         10085919_CLSTITLES
            714/699      PULSE OR DATA ERROR HANDLING
            714/724      .Digital logic testing
            714/726      ..Scan path testing (e.g., level sensitive sca
n
                           design (LSSD))
            714/731      ...Clock or synchronization

    5  714/724      (1 OR,  4 XR)
            Class   714 :  ERROR DETECTION/CORRECTION AND FAULT
                             DETECTION/RECOVERY
            714/699      PULSE OR DATA ERROR HANDLING
            714/724      .Digital logic testing

    4  324/158.1    (2 OR,  2 XR)
            Class   324 :  ELECTRICITY:  MEASURING AND TESTING
            324/158.1      MISCELLANEOUS

    3  714/732      (1 OR,  2 XR)
            Class   714 :  ERROR DETECTION/CORRECTION AND FAULT
                             DETECTION/RECOVERY
            714/699      PULSE OR DATA ERROR HANDLING
            714/724      .Digital logic testing
            714/732      ..Signature analysis

    3  714/736      (0 OR,  3 XR)
            Class   714 :  ERROR DETECTION/CORRECTION AND FAULT
                             DETECTION/RECOVERY
            714/699      PULSE OR DATA ERROR HANDLING
            714/724      .Digital logic testing
            714/736      ..Device response compared to expected
                           fault-free response

    2  327/199      (2 OR,  0 XR)
            Class   327 :  MISCELLANEOUS ACTIVE ELECTRICAL NONLINEAR
                             DEVICES, CIRCUITS, AND SYSTEMS
            327/100      SIGNAL CONVERTING, SHAPING, OR GENERATING
            327/185      .Particular stable state circuit (e.g.,
                           tristable, etc.)
            327/199      ..Circuit having only two stable states (i.e.,
                           bistable)

    2  327/202      (2 OR,  0 XR)
            Class   327 :  MISCELLANEOUS ACTIVE ELECTRICAL NONLINEAR
                             DEVICES, CIRCUITS, AND SYSTEMS
            327/100      SIGNAL CONVERTING, SHAPING, OR GENERATING
            327/185      .Particular stable state circuit (e.g.,
                           tristable, etc.)
            327/199      ..Circuit having only two stable states (i.e.,
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                         10085919_CLSTITLES
                              bistable)
           327/202            ...Master-slave bistable latch

      2   327/291            (0 OR,  2 XR)
           Class      327 :  MISCELLANEOUS ACTIVE ELECTRICAL NONLINEAR
                              DEVICES, CIRCUITS, AND SYSTEMS
           327/100            SIGNAL CONVERTING, SHAPING, OR GENERATING
           327/291            .Clock or pulse waveform generating

      2   327/299            (0 OR,  2 XR)
           Class      327 :  MISCELLANEOUS ACTIVE ELECTRICAL NONLINEAR
                              DEVICES, CIRCUITS, AND SYSTEMS
           327/100            SIGNAL CONVERTING, SHAPING, OR GENERATING
           327/291            .Clock or pulse waveform generating
           327/299            ..Single clock output with single clock input
                              or data input

      2   365/201            (0 OR,  2 XR)
           Class      365 :  STATIC INFORMATION STORAGE AND RETRIEVAL
           365/189.01         READ/WRITE CIRCUIT
           365/201            .Testing

      2   712/220            (0 OR,  2 XR)
           Class      712 :  ELECTRICAL COMPUTERS AND DIGITAL PROCESSING
                              SYSTEMS:  PROCESSING ARCHITECTURES AND    INS
TRUCTION
                              PROCESSING
           712/220            PROCESSING CONTROL

      2   714/728            (2 OR,  0 XR)
           Class      714 :  ERROR DETECTION/CORRECTION AND FAULT
                              DETECTION/RECOVERY
           714/699            PULSE OR DATA ERROR HANDLING
           714/724            .Digital logic testing
           714/726            ..Scan path testing (e.g., level sensitive sca
n
                              design (LSSD))
           714/728            ...Random pattern generation (includes
                              pseudorandom pattern)

      2   714/730            (0 OR,  2 XR)
           Class      714 :  ERROR DETECTION/CORRECTION AND FAULT
                              DETECTION/RECOVERY
           714/699.           PULSE OR DATA ERROR HANDLING
           714/724            .Digital logic testing
           714/726            ..Scan path testing (e.g., level sensitive sca
n
                              design (LSSD))
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714/730   ...Addressing

2 714/734   (0 OR, 2 XR)
       Class   714 :   ERROR DETECTION/CORRECTION AND FAULT
                            DETECTION/RECOVERY
       714/699   PULSE OR DATA ERROR HANDLING
       714/724   .Digital logic testing
       714/734   ..Structural (in-circuit test)

2 714/738   (1 OR, 1 XR)
       Class   714 :   ERROR DETECTION/CORRECTION AND FAULT
                            DETECTION/RECOVERY
       714/699   PULSE OR DATA ERROR HANDLING
       714/724   .Digital logic testing
       714/738   ..Including test pattern generator

2 714/739   (0 OR, 2 XR)
       Class   714 :   ERROR DETECTION/CORRECTION AND FAULT
                            DETECTION/RECOVERY
       714/699   PULSE OR DATA ERROR HANDLING
       714/724   .Digital logic testing
       714/738   ..Including test pattern generator
       714/739   ...Random pattern generation (includes
                            pseudorandom pattern)

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PLUS Search Results for S/N 10085919, Searched June 15, 2004

The Patent Linguistics Utility System (PLUS) is a USPTO automated search
system for U.S. Patents from 1971 to the present. PLUS is a
query-by-example search system which produces a list of patents that are
most closely related linguistically to the application searched. This
search was prepared by the staff of the Scientific and Technical
Information Center, SIRA.

6211711
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6212656
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5951702
6079040
5392296
5915084
5958075
6035431
5689517
5574731
4780874
5606565
5793778
6266041
5008618
4965511
4586057
5617427
5633606
6114892
5623503
4996691
5193092
5341096
6182256
5502731
5544173
5574733
6092226
6131173
4604746
5254942
5323400

5396170
5504756
5838693
5881067
5886901
6016564
6289477
6256770
6308291
6370664
6380724
6389567
6393592
6463561
6573703

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6211711 82
6211711 82
6212656 81
6212656 81
5951702 81
6079040 81
5392296 73
5915084 73
5958075 73
6035431 72
5689517 69
5574731 69
4780874 69
5606565 69
5793778 69
6266041 69
5008618 68
4965511 67
4586057 67
5617427 66
5633606 66
6114892 66
5623503 66
4996691 66
5193092 66
5341096 66
6182256 66
5502731 66
5544173 66
5574733 66
6092226 66
6131173 66
4604746 66
5254942 66
5323400 66
5396170 66
5504756 66
5838693 66
5881067 66
5886901 66
6016564 66
6289477 66
6256770 66
6308291 66
6370664 66
6380724 66
6389567 66
6393592 66
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6463561 66
6573703 66